Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Original) A storage method of a memory device comprising memory cells (M1 through M16) adapted to have 2^1 states for the first write operation, 2^2 states for the second write operation and $2^k = n$ states (k, n representing respective natural numbers) for the n-th write operation, said method comprising:

storing data of the first logic level or of the second logic level in data storage circuits in the k-th write operation;

modifying the state "i-1" ($I \leq n-1$, I being a natural number) of said memory cells to state "i" when the data of said data storage circuits are of the first logic level but maintaining the state of said memory cells when the data of said data storage circuits are of the second logic level;

shifting the state of said data storage circuits from the first logic level to the second logic level when the state of said memory cells has already got to state "i" and currently is at any of "0" through "i";

holding the state of said data storage circuits to the first logic level when the state of said memory cells has not got to state "i" yet and currently is at any of "0" through "i";

holding the data of said data storage circuits when the state of said memory cells is at any of "i+1" through "n-1"; and

controlling the state of said memory cells so as not to be modified from "i+1" even temporarily when the state of said memory cells is modified from "i-1" to "i".

Claims 2-20 (canceled)